2nd Proceeding of International Conference on Science and Technology UISU (ICST)
"Engineering for Suistanable Future: Innovation in Renewable Energy, Green Technology, and Circular Economy"
ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

Hardware-Implemented Multi-Agent Coordination for Adaptive Traffic Control in Developing Regions: A Low-Cost Microcontroller Approach

Hermansyah Alam[1)], Freddy Kurniawan[2),] Helma Widya[3)]
[1)]Department of Electrical Engineering, Universitas Islam Sumatera Utara, Indonesia
[2)]Department of Electrical Engineering, Institut Teknologi Dirgantara Adisutjipto, Indonesia
[3)]Dosen Politeknik LP3I Medan
Email: hermans_itm@yahoo.co.id; freddykurniawan@itda..ac.id
Correspondence Author Email: freddykurniawan@itda..ac.id

Abstract−This paper presents the design, implementation, and evaluation of a coordinated multi-agent traffic signal control system tailored for developing regions with limited infrastructure. The system employs a decentralized architecture using cost-effective microcontrollers to manage adjacent intersections, enabling local decision-making and real-time synchronization without reliance on cloud services or high-bandwidth networks. A green phase coordination algorithm was developed, leveraging timing data from a Real-Time Clock (RTC) and wireless communication at 433 MHz to synchronize green intervals between controllers. To ensure smooth traffic flow and rapid recovery from disruptions, the algorithm restricts adjustments to a maximum of 25% of the signal cycle and can restore synchronization within one to two cycles. Field trials at signalized intersections in Yogyakarta, Indonesia, demonstrate effective reduction of vehicle delays and improved adaptability to fluctuating traffic volumes. Comparative analysis with similar approaches highlights the proposed system's superior cost-effectiveness, scalability, and ease of integration with legacy infrastructure. The findings validate the system as a practical solution for sustainable traffic management in resource-constrained urban environments, supporting the broader adoption of intelligent transportation systems in developing countries.

Keywords: Coordinated, Traffic, Signal Control, Microcontroller; Management; Synchronization, Regions

1. INTRODUCTION

Traffic congestion continues to pose a significant challenge in urban areas worldwide, notably in developing countries such as Indonesia. During peak hours, ineffective traffic signal timings exacerbate congestion, resulting in prolonged travel times, increased fuel consumption, higher vehicle maintenance expenses, and elevated carbon emissions [1]. Typically, existing traffic management in developing regions predominantly relies on standalone fixed-time controllers, which lack adaptability to real-time traffic fluctuations, often causing vehicle queues to propagate across adjacent intersections [2][3]. Although alternative solutions such as public transportation expansion and road infrastructure upgrades are available, these approaches are cost-intensive and only offer short-term congestion relief [4].

To mitigate congestion economically and sustainably, optimizing traffic signal coordination emerges as a viable and cost-effective strategy. Intelligent Transportation Systems (ITS) deployed in developed countries utilize extensive sensor networks and real-time analytics for optimal traffic flow management [5][6][7]. However, these sophisticated systems are largely unsuitable for countries like Indonesia due to their considerable infrastructure demands and associated costs[8][9][10]. So that, the adoption of ITS in Indonesia is estimated to take a long time [11][12]. In contrast, coordinated traffic control systems—which synchronize signals across adjacent intersections to prioritize continuous green waves for major traffic routes—represent a pragmatic and less data-intensive solution suitable for resource-constrained settings[13].

Recent studies have made notable strides towards adaptive traffic control tailored for resource-limited environments common in developing regions. Xing et al. demonstrated through "TinyLight" that deep reinforcement learning (DRL) methods could effectively operate on microcontrollers with extremely limited resources, requiring only approximately 2 KB RAM and 32 KB ROM, presenting a viable solution for cost-sensitive hardware implementations [14]. Additionally, Mishra et al. addressed infrastructural constraints explicitly in their "CoSiCoSt" model, employing crowd-sourced traffic data and the AIMD algorithm to adaptively manage signals, proving its scalability and effectiveness in developing countries lacking comprehensive sensor networks [15]. Furthermore, recent hardware implementations, such as Zhang and Su's adaptive traffic controller using the STM32 microcontroller, have validated the feasibility of embedding intelligent signal optimization into existing low-cost systems [16]. Complementing these efforts, multi-agent reinforcement learning (MARL) approaches have shown significant performance gains, reducing fuel consumption and travel times by approximately 11% and 13%, respectively, compared to conventional fixed-time systems [17]. Despite these advancements, a critical gap remains unaddressed: existing solutions either utilize expensive hardware components, necessitate high-bandwidth communications, or fail to integrate seamlessly with legacy systems. Consequently, there remains a clear need for an affordable, scalable hardware architecture specifically designed to align with infrastructural and financial constraints prevalent in developing countries.

Collectively, the existing solutions emphasize the necessity of a scalable and cost-effective hardware architecture tailored explicitly to the infrastructural constraints that prevail in developing regions. Many current adaptive traffic signal systems either rely on high-cost hardware components or require costly upgrades to support real-time optimization, which poses barriers for integration into legacy signal controllers commonly found in

2nd Proceeding of International Conference on Science and Technology UISU (ICST)
"Engineering for Suistanable Future: Innovation in Renewable Energy, Green Technology, and Circular Economy"
ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

resource-limited settings. In addition, the need for substantial communication bandwidth and bespoke infrastructure further limits their practical implementation in wealth-constrained municipalities [18]. This underscores a clear research gap: innovative architectures are needed that balance operational performance, affordability, and compatibility with existing traffic management systems — specifically tailored for developing countries' unique infrastructural realities.

Addressing this critical research gap, this study proposes a coordinated multi-agent traffic control system specifically designed for developing nations, emphasizing optimization of vehicle flow between adjacent intersections through synchronized signal timings. The proposed architecture employs a decentralized multi-agent framework wherein each intersection autonomously manages traffic signals via cost-effective microcontrollers. This decentralized configuration enables local decision-making and real-time coordination among intersections without dependence on centralized cloud services or high-bandwidth communication infrastructures. Consequently, intersections collaboratively synchronize signal timings to establish progressive green waves, adapting effectively to real-time traffic volume fluctuations using minimal sensor data. By implementing this locally coordinated multi-agent approach, the proposed system effectively addresses infrastructural constraints and cost limitations characteristic of previous ITS solutions, making it particularly suitable for resource-constrained regions such as Indonesia.

2. RESEARCH METHODOLOGY

2.1 System Design

The research methodology employed in this study is the part of systematically integration of the design, prototyping, coordination algorithm implementation, and performance evaluation stages. Initially, the traffic signal control logic is established, featuring twelve distinct states per cycle for controlling a four-way intersection, characterized by specific green, yellow, and clearance intervals for each direction. This structured sequencing provides the foundational logic upon which the proposed traffic management system operates.

Subsequently, the research proceeds to system prototyping, utilizing a master-slave architecture consisting of two coordinated controllers placed approximately 500 meters apart, simulating adjacent intersections. The master controller functions autonomously according to a predetermined schedule, while the local controller dynamically adjusts its signal timings based on synchronization data received from the master. This architecture facilitates adaptive signal coordination and demonstrates scalability for potential future extensions without significant hardware modifications. Optimization techniques such as integer arithmetic and resource-efficient data handling are incorporated to ensure the system's efficient operation on cost-effective hardware platforms [26].

The core stage involves the implementation of a traffic coordination algorithm designed for adjusting green phase durations to maintain synchronization between intersections. The algorithm's operation relies on precise timing data obtained from a DS1307 Real-Time Clock (RTC), with scheduled signal durations stored in the microcontroller's EEPROM. At each cycle's completion, coordination data transmission from master to slave controllers is conducted via the USART protocol, employing a wireless transmission module (KYL-1020U) operating at 433 MHz. Adjustments to green times are carefully calculated to avoid exceeding 25% of the total cycle duration, ensuring smooth transitions without causing excessive disruption to traffic flow. This research further develops a previously designed coordinated traffic controller prototype specifically implemented at Gondomanan and Bintaran intersections in Yogyakarta, Indonesia, where coordination between intersections was initially established using an AVR ATmega128A microcontroller [19]. The block diagram of the enhanced system architecture proposed in this study is presented in Figure 1.

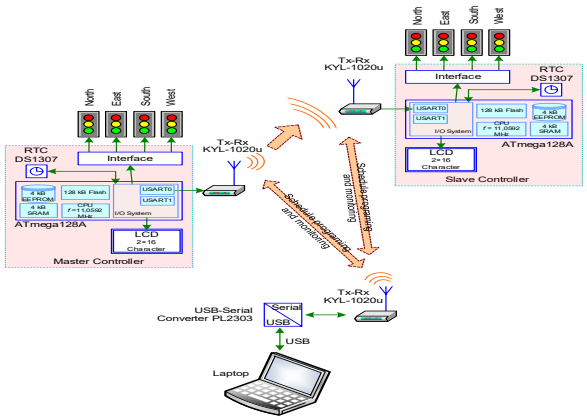


Figure 1. Block diagram of the coordinated traffic signal control system prototype

Testing and validation methods involve real-time simulations, focusing on performance metrics such as synchronization accuracy, cycle transitions, and error correction capability. Particular attention is paid to slot

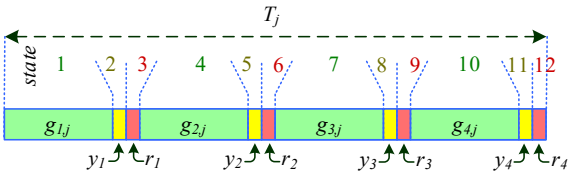
2nd Proceeding of International Conference on Science and Technology UISU (ICST)
"Engineering for Suistanable Future: Innovation in Renewable Energy, Green Technology, and Circular Economy"
ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

transition periods, during which both master and slave controllers shift between different traffic schedule time slots. Simulated scenarios include the controller's temporary deactivation, followed by a system recovery test to evaluate the algorithm's resilience and rapid synchronization recovery capabilities. Detailed analyses of these scenarios demonstrate that the proposed coordination mechanism effectively manages timing discrepancies within one to two signal cycles, thereby affirming the system's suitability for real-world deployment.

Ultimately, this structured and sequential approach, from conceptual design and hardware prototyping to algorithmic implementation and rigorous performance evaluation, ensures comprehensive coverage of the research objectives. The systematic methodology employed validates the practicality, effectiveness, and scalability of the proposed coordinated traffic control system for developing regions.

2.2 Phase Squence

Traffic signal control is based on a sequence of states. In one cycle, there are twelve states for a controller regulating a four-way intersection. When initially activated, the controller executes the control scheme starting from the first cycle. The cycle number is denoted by *j*. The sequence of states in the *j*-th cycle follows the diagram in Figure 2.



Legend:
i = Phase number
$g_{i,j}$ = Green duration of phase i in cycle j
r_i = Yellow duration of phase i
r_i = Clearance time (all-red interval) for phase i

Figure 2. Sequence of states in one cycle

In a scheduled traffic controller, the green signal duration for each phase can vary according to the predetermined schedule, while the yellow signal duration and clearance time typically remain constant. The traffic signal cycle period (T_j) follows Equation (1).

$$T_j = \sum_{i=1}^{4} (g_{i,j} + k_i + r_i) \qquad (1)$$

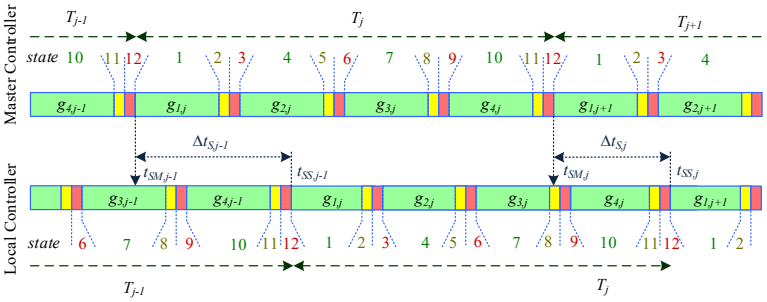
The system processor performs a countdown of each phase's signal timing every second during operation. Signal coordination is achieved by adjusting the timing offset between adjacent traffic signals. Three primary methods are employed for offset synchronization to establish coordinated conditions:

1. Dwell Method: Temporarily holding the current phase duration
2. Directional Adjustment: Increasing/decreasing green time for the coordinated direction only
3. Global Adjustment: Increasing/decreasing green time for all directions simultaneously

2.3 Coordination Process for Green Phase Duration Adjustment

The microcontroller periodically reads time data from the DS1307 Real-Time Clock (RTC). Based on this temporal data, the system determines each signal's duration according to the schedule stored in the microcontroller's EEPROM. Both Master and Local controllers regulate the traffic lights for four approach directions, with countdown timers displayed on an LCD panel.At the end of the 12th state, the Master transmits coordination data to the Local controller using the USART (Universal Synchronous/Asynchronous Receiver-Transmitter) protocol. The USART output feeds into a KYL-1020U Tx/Rx module for wireless transmission via FSK (Frequency Shift Keying) modulation at 433 MHz with 500 mW output power.

The study implements a green-time adjustment method for all approaches at the Local controller. The total duration modification for phases 1-4 must not exceed 25% of the cycle period. If calculations indicate required adjustments ≥25% of the cycle period, the coordination executes across multiple cycles.Both controllers operate according to their schedules, with EEPROM schedule updates occurring at the end of the 11th state. At the 12th state's conclusion, the Master traffic signal controller transmits synchronized data to the Local controller via USART0. The coordination reception time at the Local controller during cycle j is denoted as $t_{SM:j}$, as illustrated in Figure 3.



ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

Figure 3. Master-Local synchronization mechanism

The coordination process calculates the green phase duration adjustment for the next cycle, stored in variable $\Delta g_{i:j+1}$. This value is reset at the end of each cycle. The coordination algorithm is executed by the local controller at the end of state-12. The coordination algorithm for cycle-j operates as follows:

1. Read Real-Time Clock (RTC) data and record as slave coordination execution time: $t_{SS,j}$.
2. Calculate coordination delta: $\Delta t_{S,j} = t_{SM,j} - t_{SS,j}$
3. Determine coordination error: $\xi_j = \omega_{MS} - \Delta t_{S,j}$where ω_{MS} represents vehicle travel time from master to local controller.
4. Validate error threshold: If $\xi_j > T_j$, abort coordination and return to main program.
5. For $\xi_j > 0$: Proceed to Step 10.
6. For $\xi_j < -\frac{T_j}{4}$: Set $\xi_j = -\frac{T_j}{4}$(where ε is the maximum allowable negative error).
7. Compensate error to next cycle's green duration using Equation 2:
   $$\Delta g_{i:j+1} = \frac{g_{i:j}}{\sum_1^4 g_{i:j}} \times \xi_j \quad (2)$$
   where:
   a. $\Delta g_{i:j+1}$ = green phase duration adjustment for phase-i in cycle-(j+1)
   b. $g_{i:j}$ = current green duration for phase-i in cycle-j
8. Error zeroing: All system variables use 8-bit or 16-bit integer types. Equation 2 may not fully zero ξ_j. Residual error is distributed across phases through:
   a. Identify phase with longest green duration: $i_{h\text{-}maks} = max(g_{i:j+1})$
   b. Increment ξ_j by 1 and decrement $g_{i:j+1}$ for $i = i_{g\text{-}max}$
   c. If $\xi_j < 0$, remove $i_{g\text{-}max}$ from consideration and repeat from 8a.
9. Return to main program.
10. For $\xi_j = 0$: Return to main program.
11. For $\xi_j > \frac{T_j}{4}$: Set $\xi_j = \frac{T_j}{4}$ (maximum positive error).
12. Positive error compensation: Apply Equation 2 to all phase durations.
13. Residual positive error handling:
    a. Identify $i_{g\text{-}max} = max(g_{i:j+1})$
    b. Decrement ξ_j by 1 and increment $h_{i:j+1}$ for $i = i_{g\text{-}max}$
    c. If $\xi_j > 0$, exclude $i_{h\text{-}maks}$ and repeat from 13a.
14. Return to main program.

2.4 Modeling Assumptions

This study evaluates the performance of a developed prototype system for coordinated vehicle flow control at two adjacent signalized intersections (Fig. 2). The primary metric analyzed is the reduction in average vehicle waiting time achieved through the proposed control strategy. The simulation framework incorporates the following key parameters:

1. Intersection Configuration: Two intersections separated by 500 meters.
2. Control Architecture: Agent-based decentralized control - Agent 1 governs Intersection 1, while Agent 2 manages Intersection 2.
3. Signal Phasing: Four-phase clockwise sequencing implemented independently per intersection.
4. Movement Permissions:
   a. Green phases ($g_{m,n}$,where m = intersection index, n = phase index) permit through and right-turn movements.
   b. Left turns operate continuously under permissive mode without conflicting movements.
5. Vehicle Dynamics: Constant speed regime maintained between 40–60 km/h.

3. RESULT AND DISCUSSION

This study utilizes optimal green phase durations obtained from two four-way intersections in Yogyakarta, Indonesia: Kilometer Zero (city center) and Gondomanan. Ten distinct time slots were established for daily operational requirements. The weekday schedule for master and local controllers follows the configuration detailed in Table 1, which specifies green signal durations for both controllers and corresponding activation time windows. This schedule data is stored in the EEPROM of each microcontroller. Meanwhile, the Yellow Duration, uniformly set at 3 seconds for all approaches at both intersections and All-Red Clearance is 5 seconds for all phases

2nd Proceeding of International Conference on Science and Technology UISU (ICST)
"Engineering for Suistanable Future: Innovation in Renewable Energy, Green Technology, and Circular Economy"
ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

Table 1. The second green phase sequence for the controller

Time slot	Time	Master Controller				Local Controller				T
		g_1	g_2	g_3	g_4	g_1	g_2	g_3	g_4	
1	04:30	8	8	10	8	0	0	0	0	0
	05:00	8	8	10	8	6	8	8	9	66
2	06:00	8	15	20	15	8	10	18	19	90
3	06:30	15	25	40	30	12	15	35	45	142
4	07:10	17	25	40	30	12	17	35	45	144
5	08:30	20	28	40	30	10	25	35	45	150
6	10:00	25	28	38	30	10	25	38	45	153
7	15:30	30	28	30	30	10	25	35	45	150
8	18:00	25	25	30	25	10	21	31	40	137
9	21:30	15	15	15	15	8	15	16	18	92
10	23:00	0	0	0	0	0	0	0	0	0

3.1 Traffic Control System Based on Time Slot Coordination

Each traffic controller operates according to a predefined schedule of time slots stored in its database. When a controller transitions between time slots, this results in corresponding adjustments to its green phase durations. To maintain proper coordination between controllers, all slots sharing the same identification number must maintain identical start times, end times, and cycle periods, with the exception of the first slot which operates independently.

For the initial time slot configuration, the master controller begins operation at 04:30, allocating green times of 8 seconds, 8 seconds, 10 seconds, and 8 seconds to directions 1 through 4 respectively. The local controller starts its first slot at 05:00 with different green time allocations: 6 seconds, 8 seconds, 8 seconds, and 9 seconds for the corresponding directions. Both controllers maintain a common cycle period of 66 seconds as determined by Equation (1).

3.2 Analysis of Traffic Signal Coordination System

3.2.1 Slot Transition Analysis

The coordination during slot transitions is particularly noteworthy. As presented in Table 3, both controllers synchronize their operations during slot 2, adopting a shared cycle period of 90 seconds. The timing diagrams in Figure 4 visually demonstrate how the master and local controllers coordinate their green phase durations during the transition from slot 1 to slot 2, ensuring smooth traffic flow while maintaining system-wide synchronization. This transition mechanism represents a key feature of the proposed coordinated control system.

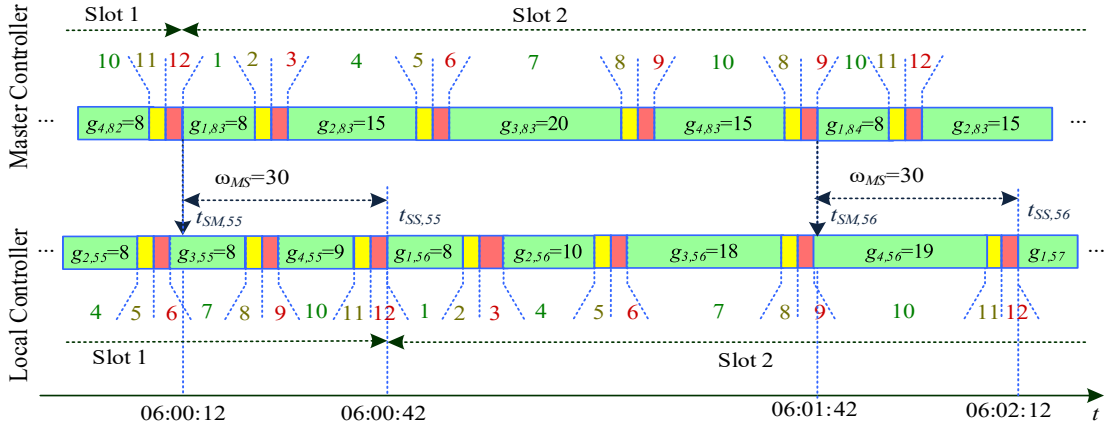


Figure 4.The coordination during slot transitions

The final cycle (82nd cycle) of slot 1 in the master controller concluded at 06:00:12, after which the controller immediately switched to slot 2. As indicated in Table 3, cycle 83 adopted a new cycle period of 90 seconds, completing at 06:01:42. At this cycle's conclusion, the master controller transmitted coordination data to the local controller, which received it as $t_{SM,56}$.

The local controller initiated slot 2 at 06:00:42. Figure 6 illustrates that its 56th cycle ended at 06:02:12, revealing a 30-second discrepancy from the master's coordination timestamp. Consequently, the coordination error $\xi_y$remained zero, demonstrating that simultaneous slot transitions between controllers can occur without introducing coordination errors.

3.2.2 Single-Cycle Coordination Recovery

A critical test case for the coordination algorithm occurs when the master controller experiences temporary deactivation, such as during power outages or maintenance, followed by reactivation. Our simulation replicated this scenario occurring at 10:00 AM. During this event, the local controller maintained operations using slot 6 (per Table

ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

2). It was executing cycle 187 (10:12:44 - 10:15:17) with T_j = 153s. The master controller reactivated at 10:12:04, also adopting slot 6 with

- Green durations: 25s (Phase 1), 28s (Phase 2), 38s (Phase 3), 30s (Phase 4)
- Synchronized cycle period: 153s

Monitoring data (Table 4) revealed an initial coordination error (ξ_j) of -10 seconds, indicating local controller timing lag. The coordination algorithm (Steps 7-8) implemented the following adjustments for cycle 188:

- Phase duration modifications: 0s (P1), -2s (P2), -4s (P3), -4s (P4)
- Resulting adjusted durations: 10s (P1), 23s (P2), 34s (P3), 41s (P4)

This single-cycle correction successfully eliminated the coordination error (ξ_j = 0) by cycle's end, demonstrating the system's capability to rapidly reestablish synchronization following controller disruptions. The transient nature of these adjustments (limited to cycle 188) confirms the algorithm's non-disruptive implementation in live traffic operations.

Table 2. Green duration when coordination occurs within one cycle

Master Controller						Local Controller										
J	g_1	g_2	g_3	g_4	T_j	J	g_1	g_2	g_3	g_4	T_j	ξ_j	$\Delta g_{1:j}$	$\Delta g_{2:j}$	$\Delta g_{3:j}$	$\Delta g_{4:j}$
-	-	-	-	-	-	187	10	25	38	45	153	0	0	0	0	0
1	25	28	38	30	153	188	10	23	34	41	143	-10	0	-2	-4	-4
2	25	28	38	30	153	189	10	25	38	45	153	0	0	0	0	0

The analysis of the coordination data reveals important findings about the system's error correction performance. At the end of cycle 187, a significant coordination error (ξ_j) of -40 seconds was observed, indicating the local controller's timing lagged behind the master controller by 40 seconds. Since this error value was below the predefined threshold - $\frac{T_j}{4}$, the coordination algorithm processed it in step 6 by adjusting ξ_j to -38 seconds (-$\frac{T_j}{4}$ value). The algorithm then calculated necessary green time adjustments for cycle 188, resulting in reductions of -2, -6, -9, and -11 seconds for phases 1 through 4 respectively. These adjustments produced modified green durations of 8, 17, 25, and 30 seconds for the corresponding phases in cycle 188. However, upon completing cycle 188, a residual error of -2 seconds remained. This remaining discrepancy was subsequently addressed in cycle 189 through compensatory adjustments to the green times, which were set to 10, 25, 37, and 44 seconds for phases 1-4 respectively. The stepwise error correction process demonstrates the system's ability to progressively eliminate timing discrepancies while maintaining operational continuity, with the complete synchronization being achieved within two operational cycles through carefully calculated phase duration modifications.

3.3 Comparison with the Other Research

The proposed hardware-implemented coordinated multi-agent traffic control system presented in this study emphasizes decentralized coordination between intersections using low-cost microcontrollers (ESP32 and Raspberry Pi). Performance evaluation demonstrates effective synchronization recovery within one to two signal cycles, with adjustments constrained below 25% of the cycle duration to minimize traffic disruption. This result aligns well with previous studies, notably the "TinyLight" system by Xing et al. [14], which successfully demonstrated adaptive signal control using microcontrollers with extremely limited resources (approximately 2 KB RAM, 32 KB ROM). However, unlike TinyLight, which employs deep reinforcement learning algorithms, our proposed approach simplifies the implementation by utilizing direct microcontroller-based signal timing adjustments without complex training or cloud computation.

Compared to the "CoSiCoSt" model by Mishra et al. [20], which adapts signal timings through crowd-sourced data and AIMD algorithms, our solution similarly addresses infrastructural constraints common in developing countries but achieves it with minimal real-time data requirements and simpler hardware configurations. Our approach's decentralized design contrasts with CoSiCoSt's reliance on external crowd-sourced traffic data, highlighting improved robustness against potential communication disruptions.

Additionally, Zhang and Su's recent adaptive traffic controller implementation using STM32 microcontrollers [16] shares similarities with our proposed method regarding the use of affordable embedded hardware platforms. Both approaches demonstrate viability for integration with legacy systems, though our system specifically incorporates wireless coordination among multiple intersections using the KYL-1020U module operating at 433 MHz, providing an effective solution for infrastructure-limited settings without extensive wired connections.

Furthermore, a comparable study by Kolat et al. employing Multi-Agent Reinforcement Learning (MARL) [17] reported reductions in fuel consumption and travel times by approximately 11% and 13% respectively. While these findings represent significant improvements over fixed-time systems, our coordinated multi-agent hardware implementation achieves synchronization and traffic optimization through predefined adaptive algorithms rather than complex MARL models, thus reducing computational overhead and resource requirements.

In conclusion, this study's results reinforce the practicality and efficiency of implementing decentralized traffic control using low-cost microcontroller-based hardware. By simplifying the coordination algorithm and minimizing infrastructural dependencies, this research extends previous work, offering a scalable, cost-effective, and resilient

ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

solution particularly suitable for developing countries like Indonesia. To further contextualize the contributions of this study, Table 1 presents a comparative analysis between the proposed system and several related traffic control approaches from recent literature. The comparison highlights key differences in control architecture, hardware platform, communication methods, and infrastructure requirements, emphasizing the unique balance of cost-effectiveness, simplicity, and scalability achieved by the proposed solution.

Table 2. The comparative analysis between the proposed system and several related traffic control approaches

Aspect	Proposed System (This Study)	TinyLight [14]	CoSiCoSt [15]	STM32-based Controller [16]	MARL-based Approach [17]
Control Architecture	Decentralized multi-agent	Decentralized single-agent	Centralized via crowd-source	Single-controller adaptive	Decentralized MARL
Hardware Platform	ESP32/Raspberry Pi	Microcontroller (low-resource, 2KB RAM, 32KB ROM)	Generic low-cost hardware	STM32 microcontroller	Higher resource microcontrollers
Communication Method	Wireless (433 MHz, KYL-1020U)	Wired/Local communication	Wireless via internet-based API	Wired/Wireless local communication	Wired/Wireless communication
Algorithm Complexity	Moderate (Adaptive synchronization)	Moderate (Light DRL algorithm)	Moderate (AIMD + crowd-data processing)	Moderate (Embedded control logic)	High (Deep Q-learning)
Sensor/ Data Requirement	Minimal sensor data (RTC-based timings)	Minimal sensor data	Extensive external crowd-source data	Moderate (local sensors)	Moderate to high sensor data
Adaptability to Legacy Systems	High (simple retrofit)	Moderate (resource constraints)	Moderate (internet required)	High (designed for embedded systems)	Moderate to low
Synchronization Recovery Speed	Fast (1–2 cycles)	Fast (real-time adaptive)	Moderate (dependent on crowd-data)	Moderate (adaptive)	Fast (real-time adaptive)
Cost-effectiveness	Very high	High	High	High	Moderate (requires higher computation)
Infrastructure Requirements	Minimal (low bandwidth wireless)	Minimal	Moderate (Internet required)	Low to moderate	Moderate to high
Main Advantage	Simple, scalable, decentralized coordination	Lightweight computation suitable for resource-limited hardware	Data-driven adaptive approach suitable for developing regions	Effective embedded adaptive control	High efficiency in traffic optimization
Main Limitation	Limited real-time adaptive capability	Single-agent limited adaptability	Reliance on stable internet/crowd data	Limited inter-intersection coordination capability	Higher computational demands

4. CONCLUSION

Based on the presented results and discussion, several conclusions can be drawn. The proposed Coordinated Traffic Signal Control System can be effectively implemented using the ATmega128A microcontroller, demonstrating its feasibility for schedule-based traffic management. The coordination mechanism between master and slave controllers is achieved by dynamically adjusting green-phase durations in the slave controller, enabling synchronization without complex infrastructure requirements. The system exhibits rapid coordination recovery, typically requiring only one to two cycles to realign signal timing after disruptions. Notably, the traffic control program operates efficiently using 8-bit and 16-bit integer variables and integer arithmetic, confirming its computational simplicity and suitability for deployment on low-cost embedded systems. These findings collectively validate the system's practicality for developing regions where resource constraints preclude sophisticated traffic management solutions.

ISSN:3063-7929 (Online)
DOI: https://doi.org/10.30743/icst

REFERENCES

[1] H. B. Faheem, A. M. El Shorbagy, and M. E. Gabr, "Impact Of Traffic Congestion on Transportation System: Challenges and Remediations - A review," *Mansoura Engineering Journal*, vol. 49, no. 2, Jan. 2024, doi: 10.58491/2735-4202.3191.

[2] H. Alam *et al.*, "Traffic Signal Timing Coordination to Minimize Vehicle Wait Times," in *Advances in Engineering Research*, F. Kurniawan, Ed., Atlantis Press, 2025, pp. 167–173. doi: 10.2991/978-94-6463-668-0_20.

[3] F. Kurniawan, D. Dermawan, O. Dinaryanto, and M. Irawati, "Pre-Timed and Coordinated Traffic Controller Systems Based on AVR Microcontroller," *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, vol. 12, no. 4, p. 787, Dec. 2014, doi: http://doi.org/10.12928/telkomnika.v12i4.497.

[4] G. Duranton and M. A. Turner, "The fundamental law of road congestion: Evidence from US cities," *American Economic Review*, vol. 101, no. 6, pp. 2616–2652, Oct. 2011, doi: 10.1257/aer.101.6.2616.

[5] F. Desimoni, S. Ilarri, L. Po, F. Rollo, and R. Trillo-Lado, "Semantic traffic sensor data: The TRAFAIR experience," *Applied Sciences (Switzerland)*, vol. 10, no. 17, Sep. 2020, doi: 10.3390/app10175882.

[6] X. Zhang, X. Fan, S. Yu, A. Shan, and R. Men, "Multi-Objective Optimization Method for Signalized Intersections in Intelligent Traffic Network," *Sensors*, vol. 23, no. 14, Jul. 2023, doi: 10.3390/s23146303.

[7] Z. Lv and W. Shang, "Impacts of intelligent transportation systems on energy conservation and emission reduction of transport systems: A comprehensive review," *Green Technologies and Sustainability*, vol. 1, no. 1, p. 100002, Jan. 2023, doi: https://doi.org/10.1016/j.grets.2022.100002.

[8] Y. Lian, G. Zhang, J. Lee, and H. Huang, "Review on big data applications in safety research of intelligent transportation systems and connected/automated vehicles," *Accid Anal Prev*, vol. 146, Oct. 2020, doi: 10.1016/j.aap.2020.105711.

[9] S. C. Rai, S. P. Nayak, B. Acharya, V. C. Gerogiannis, A. Kanavos, and T. Panagiotakopoulos, "ITSS: An Intelligent Traffic Signaling System Based on an IoT Infrastructure," *Electronics (Switzerland)*, vol. 12, no. 5, Mar. 2023, doi: https://doi.org/10.3390/electronics12051177.

[10] F. Gunes, S. Bayrakli, and A. H. Zaim, "Smart cities and data analytics for intelligent transportation systems: An analytical model for scheduling phases and traffic lights at signalized intersections," *Applied Sciences (Switzerland)*, vol. 11, no. 15, Aug. 2021, doi: 10.3390/app11156816.

[11] C. D. Diderot, N. W. A. Bernice, I. Tchappi, Y. Mualla, A. Najjar, and S. Galland, "Intelligent Transportation Systems in Developing Countries: Challenges and Prospects," in *Procedia Computer Science*, Elsevier B.V., 2023, pp. 215–222. doi: 10.1016/j.procs.2023.09.030.

[12] Y. Afrizal, "Implementation of intelligent transportation system (ITS) in Indonesia," in *Proceedings of The 5th International Conference on Informatics Engineering, Science & Technology (Incitest) 2022*, AIP Conference Proceedings, 2025, p. 040028. doi: 10.1063/5.0254901.

[13] F. Kurniawan, M. Jusoh, B. Muminov, H. Alam, D. Dermawan, and M. J. Purnomo, "Development of Coordinated Control of Vehicle Traffic Flow at Adjacent Intersection," *Aviation Electronics, Information Technology, Telecommunications, Electricals, and Controls (AVITEC)*, vol. 7, no. 1, p. 103, Feb. 2025, doi: 10.28989/avitec.v7i1.2823.

[14] D. Xing, Q. Zheng, Q. Liu, and G. Pan, "TinyLight: Adaptive Traffic Signal Control on Devices with Extremely Limited Resources," May 2022, [Online]. Available: http://arxiv.org/abs/2205.00427

[15] S. Mishra, V. Singh, A. Gupta, D. Bhattacharya, and A. Mudgal, "Adaptive traffic signal control for developing countries using fused parameters derived from crowd-source data," *Transportation Letters*, vol. 15, no. 4, pp. 296–307, Apr. 2023, doi: 10.1080/19427867.2022.2050493.

[16] L. Cai, Z. Li, Y. Zhong, P. Lin, and F. Zhang, "Design and Optimization of Intelligent Traffic Light Based on STM32 Microcontroller," in *Proceedings of the 2024 International Symposium on Integrated Circuit Design and Integrated Systems*, New York, NY, USA: ACM, Nov. 2024, pp. 119–124. doi: 10.1145/3702191.3703639.

[17] M. Kolat, B. Kővári, T. Bécsi, and S. Aradi, "Multi-Agent Reinforcement Learning for Traffic Signal Control: A Cooperative Approach," *Sustainability (Switzerland)*, vol. 15, no. 4, Feb. 2023, doi: 10.3390/su15043479.

[18] M. R. Rahman and M. M. Mamun, "Smart Traffic Signal Optimization Using Real-Time Data: A Review," Feb. 07, 2025. doi: 10.20944/preprints202502.0539.v1.

[19] F. Kurniawan and A. Setiawan Honggowibowo, "Prototipe Sistem Pengatur Isyarat Lalu-lintas Terkoordinasi untuk Simpang Empat Gondomanan dan Bintaran," *J Teknol*, vol. 7, no. 1, Jul. 2014.